Notice of Allowability	Application No.	Applicant(s)	
	10/823,291	SUZUKI, HIDEHIKO	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Ammendment filed 04, January 2006*.

2. ☒ The allowed claim(s) is/are *21,23 and 24*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Reasons For Allowance

Applicant has canceled claims 1-20, and 22.

Claims 21, 23, and 24 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 21, It is clear that Vdd is chosen to be a "high supply voltage", and thus cannot be read as an arbitrary value within the combination of Kong et al. (USPN 6,242,973) and Sanwo et al. (USPN 6,472,906). The pull-up resistor of Sanwo et al. would be part of a voltage offset circuit. However, the offset circuit does not output a value approximately equal to VDD +I1*R1, where VDD + I1*R1 is equal to the difference between a high and low voltage. Therefore claim 21 is deemed allowable.

With respect to claim 23, Kong et al. does teach a capacitor circuit, which outputs a voltage to a p-transistor and to a voltage offset circuit. Wherein the voltage offset circuit outputs a different voltage to a n-type transistor. However, Kong et al. does not teach a current mirror circuit receiving a reference voltage, and outputting a reference current to the capacitor circuit. There would be no motivation to use a current mirror to as an input to capacitor Cp, because current mirrors are designed to provide a constant current. Whereas, the circuit disclosed in Fig. 2 of Kong et al. is designed to accept a varying input signal, which a current mirror would not provide. There is no cited prior art that teaches circuit of claim 23. Thus claim 23 is deemed allowable.

With respect to claim 24, the recitation of, "regardless of the logic level at the gate of the p-type transistor, the capacitor circuit is *electrically coupled* (examiner's

italics) between the gate of the p-type transistor and the second node", makes claim 24 allowable over the cited art. It can be seen that Fig. 2 of Kong et al. teaches a *physical* coupling between the capacitor circuit Cp and M1 through the source to the drain of M4 regardless of the logic state at the gate of p-type transistor M1. However, the electrical coupling of the capacitor circuit to the gate of the p-type transistor's gate (i.e. the electrical signal present at bp coupled to the gate of M1) is not present when the IN signal is a low logic value. It can be seen in Fig. 2 that when In is low transistor M4 is off, thus there is no current (electric signal) flowing from the source to the drain of M4 to the gate of M1. Thus, Kong et al. does not teach the required "electrical coupling" of the capacitor circuit to the gate of the p-type transistor when the IN signal is low (which corresponds to a high signal at the gate of M1). There is no motivation to remove M4 as to make a direct connection to the gate of M1. There is no cited art that teaches the "electrical coupling" of Cp and M1. Thus, claim 24 is deemed allowable.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Fig.1 of Vorenkamp (USPGPN 2004/0207452) discloses a circuit with a capacitor (Cp) that outputs a voltage to a PMOS transistor (M11) that receives a current form a current mirror (M8 and M9) that receives a reference current (Ip), and a voltage offset circuit (115). However, the voltage offset circuit 115 is not coupled between the current mirror, and the capacitor. Thus, Vorenkamp does not meet the limitations of claim 23. With respect to claim 24, it can be seen that Cp is electrically coupled to the gate of M11 regardless of logic state. However, Cp is not connected to ground, therefore

Vorenkamp does not meet the required recitation of having capacitor circuit being connected to ground.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
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Art Unit 2816

TH
January 17, 2006